

Attorney's Docket No.:10559/330001/P9842/Intel Corporation

REMARKS

In view of the following remarks, reconsideration and allowance of the above-referenced application are requested.

Claims 1-24 are pending, with claims 1, 7, 13, and 22 being independent. None of the claims have been amended, and no new matter has been added.

Claims 1-24 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 6,442,678 to Arora.

Claim 1

Arora fails to teach the feature of "writing a value in the speculative commit register to an architectural register in response to the multi-cycle instruction committing," as recited in Claim 1. In one exemplary embodiment, Fig. 3 of the disclosure shows a speculative commit register (SCR) 302 coupled to an architectural register 304 via a multiplexer (306) (see pages 6-7, paragraph 19). As supported in the disclosure, "in an embodiment, results generated during the execution of non-terminal sub-instructions of an MCI in the pipeline 102 may not be written to the architectural registers until the MCI commits, which occurs when the terminal sub-instruction reaches the writeback (WB) stage" (emphasis added; see page 6 paragraph 19). So, Fig. 3 of the current disclosure shows that the last stage of the pipeline is coupled to the SCR 302, and not the architectural registers until the MCI commits when the terminal sub-instruction reaches the WB stage.

Arora fails to teach this feature of Claim 1 the value at the WB stage of the pipeline goes into the ARF 105 whether or not a terminal sub-instruction reaches the writeback (WB) stage.

Attorney's Docket No.:10559/330001/P9842;Intel Corporation

For instance, Arora teaches "an output of the architectural register file is coupled to an input of the speculative register file to update the speculative register file when a misspeculation is detected" (Abstract). Fig. 1 shows that "the result data latches of a retirement stage of the pipeline are coupled to one or more inputs to ARF 105" (Arora, Col. 3, lines 20-28). Because Arora fails to teach each and every feature of Claim 1. Applicants submit that Claim 1 should be allowed.

Furthermore, Arora teaches a different data flow for a feature of Claim 1. For example, a feature of Claim 1 states that the writing of the value in the speculative commit register is to an architectural register (Fig. 3 of disclosure; pages 6-7, paragraph 19). However, Arora teaches that "the output of ARF 105 is coupled to an input of multiplexer 109," and the output of the multiplexer is coupled to the input of the SRF 106 (Arora, Col. 3, lines 20-28). Therefore, Arora teaches a different data flow for this feature of Claim 1. Furthermore, Fig. 1 of Arora shows that the writing of the value in the speculative commit register is to either itself (via the mux 109) or to the first stage 101 of the pipeline (Arora, Col. 3, lines 20-28). For at least these reasons alone, Applicants submit that Claim 1 should be allowed.

Arora also fails to teach the feature of a multi-cycle instruction (MCI). As stated in the disclosure, "during execution of the MCI, multiple instructions may be issued from the DEC stage of the pipeline 102 over several clock cycles. The MCI remains stalled in the decode stage of the pipeline 102 while multiple 'sub-instructions' may be send down the pipeline 102 (page 4, paragraph 4)." Instead, Arora teaches that an instruction can be "retired" after "the processor has finished executing an instruction and has ensured that all prior instructions will also complete" (Col. 1, lines 30-32). Arora

Attorney's Docket No.:10559/330001/P9842/Intel Corporation

states that the instructions are retired in the writeback (WB) stage (Col. 1, lines 34-39). Arora states that the results of the "retirement stage of the pipeline are coupled to one or more inputs to ARF 105" (Col. 3, lines 21-22). This is not the same as teaching the feature of multi-cycle instructions with respect to Claim 1 because terminal and non-terminal instructions/sub-instructions are handled differently for multi-cycle instructions, as described above (e.g., "writing a result generated in response to a sub-instruction in a speculative commit register," Claim 1; and "when a non-terminal instruction reaches the WB stage, any results may be written to the SCR 302 rather than an architectural register 304." page 6, paragraph 19). This is also not the same as teaching the feature of a multi-cycle instruction (MCI) as described above with respect to Claim 1 (e.g., multiple instructions issued from the DEC stage of the pipeline 102 over several clock cycles). Because at least Arora does not teach multi-cycle instructions (MCI) with respect to the features of Claim 1, Applicants submit that Claim 1 should be allowed.

Claims 2-6

Applicants submit that Claims 2-6 are allowable because they depend from an allowable base claim, Claim 1, and are allowable for reciting allowable subject matter in their own right. Allowance of Claims 2-6 is respectfully requested.

Claims 7, 13, and 22

Claims 7, 13, and 22 recite one or more features that are similar to Claim 1, and are allowable for at least the same reasons as those of Claim 1.

Claims 7, 13, and 22 are further allowable for reciting allowable subject matter in their own right. For example, Claims 13 and 22 recite "a controller operative to control writing a result from the speculative commit register to the

Attorney's Docket No.:10559/330001/P9842/Intel Corporation

architectural register in response to the terminal sub-instruction committing." As noted above with respect to Claim 1, Arora fails to teach or suggest a data flow for writing a result from the speculative commit register to the architectural register. Because Arora fails to show a data flow as described in Claim 1, Arora cannot show a controller operative for such a data flow. Therefore, Arora fails to anticipate each and every feature of Claims 13 and 22, and the 35 U.S.C. 102(b) rejections to those claims should be respectfully withdrawn.

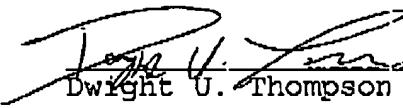
Claims 8-12, 14-21, and 23-24

Applicants submit that Claims 8-12, 14-21, and 23-24 are allowable because they depend from an allowable base claim (Claim 7 for Claims 8-12; Claim 13 for claims 14-21; Claim 22 for Claim 23-24), and are allowable for reciting allowable subject matter in their own right. Allowance of Claims 8-12, 14-21, and 23-24 is respectfully requested.

No fee is believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 06/18/04


Dwight U. Thompson
Reg. No. 53,688
Agent for Intel Corporation

Fish & Richardson P.C.
PTO Customer Number: 20985
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10402331.doc